**EXPERIMENT NO. 7**

**Program :**

module dec38(i,o);

input[2:0]i;

output[7:0]o;

reg[7:0]o;

integer n;

always @(i)

begin

for(n=0;n<=7;n=n+1)

begin

if(i==n)

o[n]=1;

else

o[n]=0;

end

end

endmodule

**Testbench**

`timescale 1ns/1ps

module dectest\_V;

reg[2:0]i;

wire[7:0]o;

dec38 dl(i,o);

initial

begin

#50 i=3'b000;

#50 i=3'b001;

#50 i=3'b010;

#50 i=3'b011;

#50 i=3'b100;

#50 i=3'b101;

#50 i=3'b110;

#50 i=3'b111;

end

endmodule

RTL SCHEMATIC :



TECHONOLGY SCHEMATIC :



Output :



=========================================================================

\* Final Report \*

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Final Results

RTL Top Level Output File Name : dec38.ngr

Top Level Output File Name : dec38

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : YES

Target Technology : Automotive 9500XL

Macro Preserve : YES

XOR Preserve : YES

Clock Enable : YES

wysiwyg : NO

Design Statistics

# IOs : 11

Cell Usage :

# BELS : 23

# AND2 : 6

# AND3 : 5

# INV : 12

# IO Buffers : 11

# IBUF : 3

# OBUF : 8

=========================================================================

CPU : 1.34 / 1.45 s | Elapsed : 2.00 / 2.00 s

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Total memory usage is 130424 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)